Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow

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ABSTRACT

Placement is among the most critical steps in analog/mixed-signal (AMS) circuit layout synthesis. It implicitly determines the wiring topology and therefore has considerable impacts on post-layout parasitics and coupling. Existing analog placement techniques are mainly focusing on geometric constraints in analog building blocks. However, there yet lacks an effective way to consider the system-level signal flow for sensitive AMS circuits. Leveraging prior knowledge from schematics, we propose to consider the critical signal paths in automatic AMS placement and present an efficient framework. Experimental results demonstrates the efficiency and effectiveness of our proposed framework with 22.8% reduction in routed wirelength compared to state-of-the-art AMS placer and 10 dB improvement in signal-to-noise-and-distortion ratio (SNDR) for an ADC.

1 INTRODUCTION

Implementing analog/mixed-signal (AMS) circuits layouts is a heavily manual, time-consuming, and error-prone task. Unlike its counterpart in the digital domain, AMS circuits are sensitive to layout parasitics and coupling while there yet lacks a practical approach to model the performance from layouts [21]. The gap in performance between schematic design and layouts poses a difficult challenge to automating the AMS layout synthesis.

In a typical automatic AMS layout synthesis flow, the placement step places the devices and macros on the layout. Placed modules are usually fixed in the following routing step; therefore, placement implicitly decides the flow of signals and currents even before the routing stage. A common approach to estimate the wiring topology in AMS placement is through wirelength models, such as half-perimeter wirelength (HPWL). However, the hyper-edge net models often underestimate the importance of the directions of signals. Unlike typical digital designs, AMS circuits are sensitive to small perturbation and distortion on the signal and therefore raise more considerable challenges on the layouts.

Regularizing the flow of critical signals is crucial for mixed-signal systems. A circuit, such as an analog-to-digital converters (ADC), often has a targeting transfer function for signals determined in the schematic design stage, specifying the resistance and capacitance along the forward and feedback loop. However, parasitic RC and couplings from layout can change the ideal behavior in frequency response and hence the degradation in post-layout performance. A common practice for manual layout design is to implement layouts according to the natural flows of critical signals in schematics and avoid detours on the signal paths. Such heuristic often results in an ideal floorplan for the overall circuit performance. Figure 1 shows a third-order continuous-time ΔΣ modulator (CTDSM) ADC. This CTDSM design has one pair of forward differential signal paths and two pairs of backward feedback signal paths, as marked in Fig. 1. Figure 1(b) and (c) are two floorplans for the CTDSM. Between them, (b) is a **place-like-schematic** placement and (c) has irregular signal paths. Although the placement in Fig. 1(c) in fact has lower **routed wirelength** than the placement, (b) is overall preferred for better **performance**. In fact, similar scenarios has been observed in recent efforts of automating system-level AMS circuit layout synthesis [22].

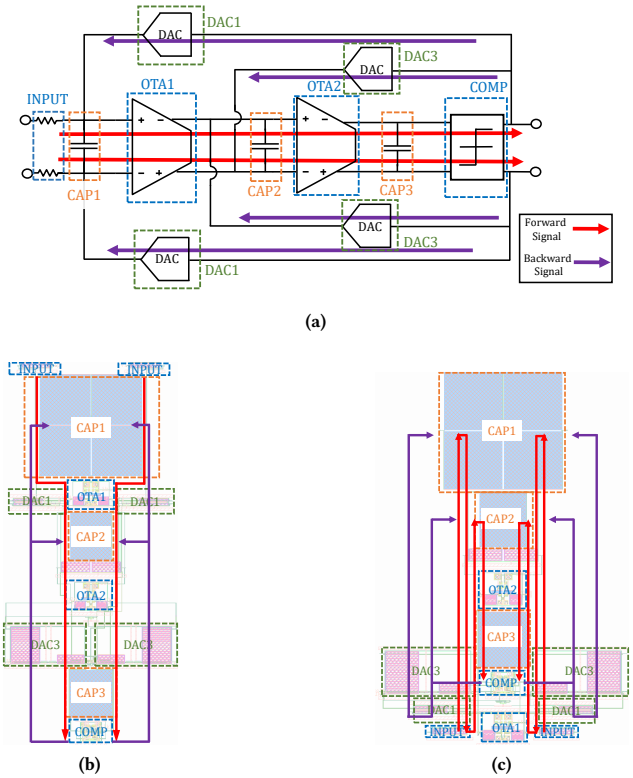

Figure 1: A third-order CTDSM. (a) Schematic. (b) Placement with regular signal flow. (c) Placement with irregular signal flow. The feedback and backward signal flows are marked in red and purple respectively in (b) and (c).

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Several existing efforts have considered the signal and current planning issues in AMS layout synthesis. The work [23] proposes a signal-path driven partition and placement for analog circuits. It traverses the circuit devices from input signals and partitions the circuits into *core-* and *bias-* circuits. After the partition, it firstly places the core-circuit following pre-defined patterns and stochastically places the rest. This methodology is efficient for certain types of block-level analog design following the *core+bias* design paradigm. However, it is difficult to be applied to other types of circuits. Another similar problem is the current flow-related constraints [28, 31, 36, 37]. In those works, the direct current from the supply (VDD) to the sink (VSS) are constrained to be monotonic in one direction. Such formulations are effective in building blocks where monotonic current flow is a widely-accepted paradigm in manual layouts. However, such constraints are not easy to be extended to general signals and system-level circuits.

In this work, we propose a new formulation of signal flow that considers the regularity of critical signal paths in mixed-signal systems and present a holistic analytical AMS placement framework. We leverage the prior knowledge of the signal paths from schematic to consider system signal flows in non-linear programming-based (NLP) global placement. The main contributions are summarized as follows.

- We propose an AMS placement framework considering system signal flows for mixed-signal circuits. The source code [1] is released on GitHub.
- We propose techniques in NLP-based global placement to improve its quality and efficiency, leveraging the prior knowledge of power/ground routing in analog layouts.
- We propose a holistic method to update the parameters and multipliers, which controls the balance between different objectives and penalties in a self-adaptive manner.
- Experimental results demonstrate that our proposed placement framework achieves better post-layout performance and placement metrics over the state-of-the-art AMS placement algorithm for a variety of benchmark circuits.

The rest of this paper is organized as follows. Section 3 introduces the preliminaries and the problem formulation. Section 4 details our AMS placement framework. Section 5 shows the experimental results, and Section 6 concludes the paper.

2 RELATED WORK

Analog placement has been a fruitful field for decades. Traditionally, the analog placement problem is formulated similar to digital floorplan problem with additional geometric constraints. The most widely-used type of constraints are the variations of symmetry constraint [1–4, 6–8, 14–20, 23–26, 28–41], which enforce certain cells to be placed symmetrically. Similar constraints on enforcing the placed locations of matched cells include common-centroid [19, 33, 38], regularity [7, 26, 39], proximity [6, 18, 25, 33–35, 41] and etc. Constraints such as monotonic current flow [28, 31, 36] and thermal effects [19, 20] have also been studied to ensure circuit performance. To ensuring the placement solutions can fit to the design floorplan, boundary constraint [14, 24, 25, 34, 35], pre-placed constrains [24, 25, 34, 35] and etc. are sometimes considered. Other work improves the manufactorability [6, 24, 29] and routability [7, 15, 28] in AMS placement problem.

Common objectives for AMS placement include area [2–4, 6–8, 14–18, 24–26, 28, 30–33, 35, 38, 39, 41], wirelength [6–8, 14, 15, 17–20, 24–26, 28, 32, 33, 35, 36, 38, 41] and etc. As the functionalities of nets differ in AMS circuits, several efforts are made to distinguish the nets. For example, the work [41] gives higher weights on the critical nets, and the work [31] tries to minimize the width and length for parallel current paths.

Stochastic approach is a classical paradigm on solving AMS placement problems such as the work of [1–4, 6–8, 14–20, 24–26, 28–32, 34–36, 38]. They usually represent layouts with designed data structure and perform randomized algorithms, such as simulated annealing, for optimization. Such paradigm is often effective but lacks direct ways to optimize the objectives. Other used solving algorithms include mixed-integer-programming (MILP) [39, 41] and non-linear programming (NLP) [29, 40]. MILP and NLP provide direct approach on optimizing the objectives such as area and wirelength. However, MILP is limited to linear objective and constraints and its scalability is concerned. On the other hand, NLP is suitable to optimize a much wider range of objective functions and is in theory has advantages in scalability. However, NLP needs to relax the constraints and therefore requires extra post-processing step to legalize the results.

3 PRELIMINARIES

In this section, we introduce the definition of system signal flow and formulate the signal flow-aware AMS placement problem.

3.1 System Signal Flow

System signal flow specifies the paths that the critical signals flowing through. This formulation differs from the critical nets in the sense that 1) the signal flow paths are crossing over different nets, and 2) pin-to-pin connection is considered rather than modeling nets as hyper-edges in the conventional approach. In this work, we introduce system signal flow as one of the objectives in global placement that results in less detours in signal paths after routing.

The system signal flow is represented as a set of paths $\mathcal{P}^{SSF}$. Each path $\mathcal{P}_i^{SSF}$ consists of a list of pins that the critical signals flow through. Within the experiments of this paper, each system-level circuit is specified with the forward and backward signal paths following the guidance from experienced circuit designers.

3.2 Problem Formulation

The signal flow-aware AMS placement problem can be formulated as follows. Given a set of modules $\mathcal{M}$, a set of pins $\mathcal{P}$, a set of nets $\mathcal{N}$, a set of power/ground nets $\mathcal{N}^{PG} \subseteq \mathcal{N}$, a set of symmetric module pairs $\mathcal{M}^{SP}$, a set of self-symmetric modules $\mathcal{M}^{SS}$, and a set of system signal flow paths $\mathcal{P}^{SSF}$, determine the coordinates of all modules considering the system signal flow such that no modules are overlapped, all the symmetric module pairs and self-symmetric modules are placed symmetrically or self-symmetrically along a certain symmetry axis. Table 1 lists the symbols used for the problem formulation.

4 ALGORITHMS

In this section, we present the proposed framework. Figure 2 shows the overall flow of our placement framework. We follow the paradigm from [40] of non-linear programming-based (NLP) global placement with linear-programming-based (LP) legalization. In the global placement stage, we spread the modules considering the placement objectives and the constraint penalties using gradient descent-based optimization. After determining the positional relationship between modules, we use LP-based techniques to legalize the layout for minimizing the area and wirelength.

[1] https://github.com/krzhu/IdeaPlaceEx

Table 1: Notations used for problem formulations.

Symbol	Description
$\mathcal{M}$	The set of modules specified in the circuit netlist
m_i	The i^{th} module in $\mathcal{M}$, $1 \le i \le \lvert\mathcal{M}\rvert$
$\mathrm{W}_i/\mathrm{H}_i$	The width/height of m_i
(x_i, y_i)	The coordinate of the bottom-left corner of m_i
$\mathcal{N}$	The set of nets specified in the circuit netlist
n_i	The i^{th} net in $\mathcal{N}$
$\mathcal{N}^{PG}$	The set of nets of power or ground
$\mathcal{P}$	The set of pins specified in the circuit netlist
p_i	The i^{th} pin in $\mathcal{P}$, $1 \le i \le \lvert\mathcal{P}\rvert$
$(\mathrm{X}_i, \mathrm{Y}_i)$	Location offset of p_i with respect to the bottom-left corner of the module containing the pin
$\mathcal{M}^{SP}/\mathcal{M}^{SS}$	The set of symmetric pair/ self-symmetry constraints
$\mathcal{P}^{SSF}$	The set of system signal flow paths
$\mathcal{P}_i^{SSF}$	The i^{th} path in $1 \le i \le \lvert\mathcal{P}^{CRF}\rvert/\lvert\mathcal{P}^{SSF}\rvert$
$p_{i,k}^{SSF}$	The k^{th} pin in $\mathcal{P}_i^{SSF}$, $1 \le k \le \lvert\mathcal{P}_i^{SSF}\rvert$
w_i^{NET}/w_i^{SSF}	The weight for $n_i/\mathcal{P}_i^{SSF}$

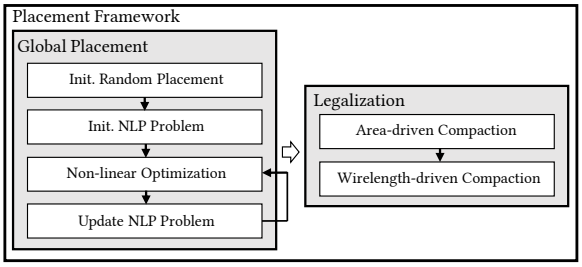


Figure 2: The overall flow of our placement framework.

In the rest of this section, the details of the global placement (Sec. 4.1) and the legalization (Sec. 4.2) will be presented.

4.1 Global Placement

Table 2: Abbreviations for the objectives and penalties.

Abbreviations	Description
SWL	Signal nets wirelength
PWL	Power and ground nets wirelength
SSF	System signal flow
CRF	Current flow
OVL	Overlapping
ASYM	Asymmetry

Algorithm 1 Global Placement

1: Initialize random placement
2: Initialize $\boldsymbol{\lambda}$ and $\boldsymbol{\gamma}$
3: **while** $\sum_{i=1}^{|\mathcal{M}|}\sum_{j=i+1}^{|\mathcal{M}|} O_{i,j}^{OVL} \ge 0.01$ or $O^{ASYM} \ge 0.05$ **do**
4: ADAM Optimization
5: Update $\boldsymbol{\lambda}$ and $\boldsymbol{\gamma}$

Global placement spread the modules in the layout, considering a variety of objectives and constraints simultaneously. Table 2 lists the objectives and penalties we consider in global placement.

Algorithm 1 shows the steps in the global placements. The design is firstly scaled down such that the total cell area is always a constant $Area_{total}$. This step ensures the numerical scale is within a suitable range, fitting the same set of hyper-parameters. $Area_{total}$ is set to 100 in the experiments. Then the locations of modules are randomly initialized. The x- and y- coordinates of modules are independently sampled from $\mathcal{N}(0, 0.01 \cdot Area_{total})$.

After initializing the placement, we then initialize the penalty multipliers $\boldsymbol{\lambda} = (\lambda_{PWL}, \lambda_{SSF}, \lambda_{CRF}, \lambda_{OVL}, \lambda_{ASYM})^T$ and the control parameters $\boldsymbol{\gamma} = (\gamma_{OVL}, \gamma_{CRF})^T$ used in log-sum-exponential (LSE) function [27]. Then, the placement enters the core optimization stage. Global placement engine iteratively optimizes the current problem and updates $\boldsymbol{\lambda}, \boldsymbol{\gamma}$. The $\boldsymbol{\lambda}$ updating scheme balances the objectives and gradually emphasizes more on hard constraints after each iteration. After both the overlapping and asymmetry are within threshold, the global placement terminates, and the design scale is recovered.

The overflows for the non-overlapping and symmetric constraints are defined as follows. The overlapping overflow is defined as pairwise overlapping area similar to [12], as shown in Equation 1.

$$\begin{aligned} O^{OVL} &= \sum_{m_i \in \mathcal{M}} \sum_{m_j \in \mathcal{M}\setminus\{m_i\}} O_{i,j}^{OVL,x} \cdot O_{i,j}^{OVL,y} / Area_{total}, \\ O_{i,j}^{OVL,x} &= \max(\min(x_i + \mathrm{W}_i - x_j, x_j + \mathrm{W}_j - x_i), 0), \\ O_{i,j}^{OVL,y} &= \max(\min(y_i + \mathrm{H}_i - y_j, y_j + \mathrm{H}_j - y_i), 0). \end{aligned} \tag{1}$$

Essentially, O^{OVL} measures the ratio of the overlapped area to the $Area_{total}$. The overlapped area is required to be below 1% of $Area_{total}$ when global placement terminates. The asymmetry overflow is defined as the average distance each symmetric-pair or self-symmetric constraints deviated from the symmetry. Assuming the symmetry axis is vertical, the definition of the asymmetry overflow is shown in Equation 2.

$$\begin{aligned} O^{ASYM} &= (\sum_{\mathcal{M}_k^{SP} \in \mathcal{M}^{SP}} O_k^{SP} + \sum_{m_i \in \mathcal{M}^{SS}} O_i^{SS}) / (|\mathcal{M}^{SP}| + |\mathcal{M}^{SS}|), \\ O_k^{SP} &= |x_i + \mathrm{W}_i + x_j - 2 \cdot x_{sym}| + |y_i - y_j| \qquad m_i, m_j \in \mathcal{M}_k^{SP}, \\ O_i^{SS} &= |x_i + \frac{1}{2} \cdot \mathrm{W}_i - x_{sym}|, \end{aligned} \tag{2}$$

where x_{sym} denotes the x-coordinate of the symmetry axis. We require O^{ASYM} below 0.05 when global placement terminates.

In the rest of Section 4.1, the details of global placement are presented.

4.1.1 The NLP Problem Formulation. In the global placement, we intend to solve the minimization problem

$$\begin{aligned} &\min_{\boldsymbol{x},\boldsymbol{y}} \ f^{WL}(\boldsymbol{x},\boldsymbol{y}) + f^{SSF}(\boldsymbol{x},\boldsymbol{y}), \\ &s.t. \ \ O^{OVL}, O^{ASYM} = 0, \end{aligned} \tag{3}$$

where $(\boldsymbol{x},\boldsymbol{y})$ denotes the current placement, f^{WL} is the weighted sum of wirelength for all nets, and f^{SSF} is the weighted sum of system signal flow cost.

Constraints (OVL and ASYM) in Equation 3 are relaxed and penalized. We further add additional penalty cost of current flow (CRF) to encourage the convergence leveraging the prior knowledge on current supply structure. We separate the signal wirelength cost and P/G wirelength cost for better wirelength estimations. After further adding multipliers to each type of the cost, our NLP problem

is formulated as a minimization problem in Equation 4.

$$\begin{aligned}\min_{\boldsymbol{x},\boldsymbol{y}}\ f(\boldsymbol{x},\boldsymbol{y}) &= \lambda_{SSF}\cdot f^{SSF}(\boldsymbol{x},\boldsymbol{y})\\ &+f^{SWL}(\boldsymbol{x},\boldsymbol{y})+\lambda_{PWL}\cdot f^{PWL}(\boldsymbol{x},\boldsymbol{y})\\ &+\lambda_{CRF}\cdot\Phi^{CRF}(\boldsymbol{x},\boldsymbol{y})\\ &+\lambda_{OVL}\cdot\Phi^{OVL}(\boldsymbol{x},\boldsymbol{y})+\lambda_{ASYM}\cdot\Phi^{ASYM}(\boldsymbol{x},\boldsymbol{y}),\end{aligned} \tag{4}$$

where λ_*, f^* and Φ^* denote multipliers, objective costs, and penalty costs respectively. In the rest of Section 4.1.1, we will presents their details.

SSF: A major motivation for this work is to honor the critical signal flow in the placement and producing floorplans similar to the human approach as shown in the examples in Figure 1. While motivated to reduce detours in a path, we intend to formulate the system signal flow in an unconstrained manner instead of fixing to certain floorplan pattern. Therefore we propose the objective f^{SSF} to quantify the degree of being straight for a signal path. Figure 3 shows the simplest signal path consisting of three modules. We formulate the SSF cost based on the angle θ between the two vectors of pins, as shown in Figure 3(a). The cost is defined as $1-\cos(\theta)$, and this cost mapping the angle smoothly to $[0,1]$. The cost with respect to $(\boldsymbol{x},\boldsymbol{y})$ for the path $m_i\rightarrow m_j\rightarrow m_k$ can be calculated as

$$\begin{aligned}1-\cos(\theta) &= 1-\frac{\vec{\mathbf{v}}_{i,j}\cdot\vec{\mathbf{v}}_{j,k}}{\left\|\vec{\mathbf{v}}_{i,j}\right\|\cdot\left\|\vec{\mathbf{v}}_{j,k}\right\|},\\ \vec{\mathbf{v}}_{i,j} &= \begin{pmatrix}x_j-x_i\\ y_j-y_i\end{pmatrix}.\end{aligned} \tag{5}$$

When extending the cost in Equation 5 to general system signal paths, we consider not only the neighboring modules along the path but also the overall regularity of the whole path. For each pair of the modules m_i, m_j along the path, we choose a module m_k in the middle of m_i, m_j from the path and add the cost for $m_i\rightarrow m_k\rightarrow m_j$ to the total cost as shown in Equation 6.

$$\begin{aligned}f^{SSF}(\boldsymbol{x},\boldsymbol{y}) &= \sum_{\mathcal{P}_i^{SSF}\in\mathcal{P}^{SSF}} w_i^{SSF} f_i^{SSF}(\boldsymbol{x},\boldsymbol{y}),\\ f_i^{SSF}(\boldsymbol{x},\boldsymbol{y}) &= \sum_{j=1}^{|\mathcal{P}_i^{SSF}|-2}\ \sum_{k=j+2}^{|\mathcal{P}_i^{SSF}|} f^{SSF}_{i,j,k,\lfloor(j+k)/2\rfloor},\\ f^{SSF}_{i,j,k,l} &= 1-\frac{\vec{\mathbf{v}}^{\,i}_{j,l}\cdot\vec{\mathbf{v}}^{\,i}_{l,k}}{\left\|\vec{\mathbf{v}}^{\,i}_{j,l}\right\|\cdot\left\|\vec{\mathbf{v}}^{\,i}_{l,k}\right\|},\\ \vec{\mathbf{v}}^{\,i}_{j,k} &= \begin{pmatrix}x_k^{i,*}-x_j^{i,*}\\ y_k^{i,*}-y_j^{i,*}\end{pmatrix},\end{aligned} \tag{6}$$

where $(x_j^{i,*}, y_j^{i,*})$ denotes the coordinates of the module containing the j^{th} pin of the path $\mathcal{P}_i^{SSF}$ and $\lfloor\rfloor$ is the floor function. $\lfloor(j+k)/2\rfloor$ is to indicate a module in the middle of i^{th} and k^{th} pins on the path. We omit the offset of pin location offsets in Equation 6 for simplicity.

SWL: We choose to model the wirelength of signal nets using the widely-used half-perimeter wirelength (HPWL),

$$HPWL(\boldsymbol{x},\boldsymbol{y}) = \sum_{n_i\in\mathcal{N}\setminus\mathcal{N}^{PG}}\left(\max_{m_j,m_k\in n_i}|x_j-x_k|+\max_{m_j,m_k\in n_i}|y_j+-y_k|\right), \tag{7}$$

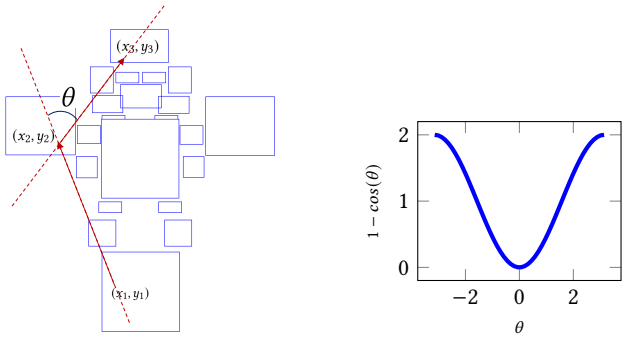


Figure 3: System signal flow objective. (a) a three-module signal path. (b) The plot of function $1-\cos(\theta)$.

We approximate Equation 7 with the log-sum-exponential (LSE) function [27], as shown in Equation 8.

$$\begin{aligned}f^{SWL}(\boldsymbol{x},\boldsymbol{y}) &= \sum_{n_i\in\mathcal{N}\setminus\mathcal{N}^{PG}} w_i^{NET}\cdot\left(f_{i_x}^{SWL}(\boldsymbol{x},\boldsymbol{y})+f_{i_y}^{SWL}(\boldsymbol{x},\boldsymbol{y})\right),\\ f_{i_x}^{SWL}(\boldsymbol{x},\boldsymbol{y}) &= \log\sum_{m_j\in n_i}(e^{x_i})+\log\sum_{m_j\in n_i}(e^{-x_i}),\\ f_{i_y}^{SWL}(\boldsymbol{x},\boldsymbol{y}) &= \log\sum_{m_j\in n_i}(e^{y_i})+\log\sum_{m_j\in n_i}(e^{-y_i}).\end{aligned} \tag{8}$$

We omit the offset of pin location offsets in Equation 7 and Equation 8 for simplicity.

PWL: In analog layout design, the power and ground (PG) nets are often routed in a different approach from the signals. As shown in the example of Figure 4, the pins of PG nets are more likely to be individually connected to the current supply/sink. Besides, the current supply/sink is reasonably wide to cover the boundary of the placement. Therefore we propose to use a different wirelength model for the PG nets such that 1) pins are considered separately instead of being modeled as in a net-wise hyper-edge, and 2) only the vertical distance to the current supply/sink is considered. Equation 9 shows the defination.

$$f^{PWL}(\boldsymbol{x},\boldsymbol{y}) = \sum_{n_i\in\mathcal{N}^{PG}} w_i^{NET}\cdot\sum_{m_j\in n_i}(y_j-\mathrm{Y}_{P/G})^2, \tag{9}$$

where $\mathrm{Y}_{P/G}$ is the estimated y-coordinate of the current supply/sink. Y_P and Y_G are set to be placed slightly above or beneath the estimated boundary of the placement correspondingly and is updated in each iteration if the placement exceed the previous estimated boundary.

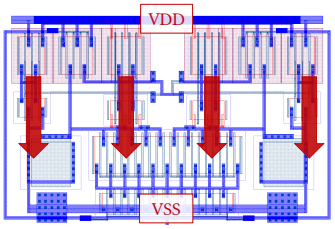


Figure 4: An example of current supply structure in manual comparator layout.

CRF: We propose a current flow penalty for the sake of convergence and layout quality. As discussed above, the prior knowledge of the current supply structure and P/G routing can be leveraged in

the placement engine. Modules along the current paths are likely to be placed following the current direction. Inspired by the work [37], we propose to penalize non-monotonic current flow in the global placement. By giving preference on monotonic current flow to the NLP problem, we observe improvements on NLP convergence and benefits in P/G routing after placement in our experiments. We define the violation or overflow of monotonic current flow as Equation 10.

$$\begin{aligned} O^{CRF} &= \sum_{\mathcal{P}_i^{CRF} \in \mathcal{P}^{CRF}} O_i^{CRF}, \\ O_i^{CRF} &= \sum_{k=1}^{k \le |\mathcal{P}_i^{CRF}|-1} \max(y^*_{i,k+1} - y^*_{i,k}, 0), \end{aligned} \tag{10}$$

where $y^*_{i,j}$ denotes the y-coordinate of the module containing the j^{th} pin in the path $\mathcal{P}_i^{CRF}$. Equation 10 is further smoothed with LSE function as Equation 11.

$$\begin{aligned} \Phi^{CRF}(\boldsymbol{x}, \boldsymbol{y}) &= \sum_{\mathcal{P}_i^{CRF} \in \mathcal{P}^{CRF}} w^{CRF} \cdot \phi_i^{CRF}, \\ \phi_i^{CRF} &= \sum_{k=1}^{k \le |\mathcal{P}_i^{CRF}|-1} LSE(y^*_{i,k+1} - y^*_{i,k}), 0, \gamma_{CRF}), \\ LSE(x, y, \gamma) &= \gamma \cdot \log(e^{x/\gamma} + e^{x/\gamma}), \end{aligned} \tag{11}$$

where γ_{CRF} is a parameter to control the smoothness and accuracy of the LSE approximation, $y^*_{i,j}$ denotes the y-coordinate of the module containing the j^{th} pin in the path $\mathcal{P}_i^{CRF}$ and w^{CRF} is the weight for each segment in the paths. We set w^{CRF} to 0.5 for all segments in the experiments. We omit the pin offsets from Equation 11 for simplicity.

OVL: The overlapping penalty is the smoothed version of Equation 1. We approximate the max and min with LSE and obtain Equation 12.

$$\begin{aligned} \Phi^{OVL}(\boldsymbol{x}, \boldsymbol{y}) &= \sum_{m_i, m_j \in \mathcal{M}} \phi_{i,j}^{OVL}, \\ \phi_{i,j}^{OVL}(\boldsymbol{x}, \boldsymbol{y}) &= LSE(LSE(x_i + \mathrm{W}_i - x_j, x_j + \mathrm{W}_j - x_i, -\gamma_{OVL}), 0, \gamma_{OVL}), \\ LSE(x, y, \gamma) &= \gamma \cdot \log(e^{x/\gamma} + e^{x/\gamma}), \end{aligned} \tag{12}$$

where γ_{OVL} is a parameter to control the trade-off between smoothness and accuracy in LSE approximations.

ASYM: The asymmetry penalty is the smoothed version of Equation 2 by squaring the absolute functions, as shown in Equation 13.

$$\begin{aligned} \Phi^{ASYM}(\boldsymbol{x}, \boldsymbol{y}) &= \Big(\sum_{\{m_i, m_j\} \in \mathcal{M}^{SP}} \phi_{i,j}^{SP} + \sum_{m_i \in \mathcal{M}^{SS}} \phi_i^{SS} \Big) / (|\mathcal{M}^{SP}| + |\mathcal{M}^{SS}|), \\ \phi_{i,j}^{SP}(\boldsymbol{x}, \boldsymbol{y}) &= (x_i + \mathrm{W}_i + x_j - 2 \cdot x_{sym})^2 + (y_i - y_j)^2 \\ \phi_i^{SS}(\boldsymbol{x}, \boldsymbol{y}) &= (x_i + \frac{1}{2} \cdot \mathrm{W}_i - x_{sym})^2, \end{aligned} \tag{13}$$

where x_{sym} denotes the x-coordinate of the symmetry axis.

4.1.2 ADAM Optimization. We feed the NLP problem in each iteration to an optimization kernel based on ADAM optimizer [11]. Algorithm 2 shows the details of the optimization kernel, where α is the step size for Adam optimizer, β_1, β_2 are the exponential decay rates for the moment estimates, δ is the step size for vanilla gradient descent, t_{GD} denotes after which iteration we switch to vanilla gradient descent from Adam optimizer and ϵ is a small number for avoiding divide-by-zero. Line 7-11 is the standard ADAM optimizer algorithm. The optimization process is accelerated through estimating the first and second moments of the gradients. When the optimization is slow to converge, we switch to vanilla gradient descent with a small step size to search for a nearby local minima (line 14). We set $\alpha = 0.005$, $\beta_1 = 0.9$, $\beta_2 = 0.999$, $\epsilon = 10^{-8}$, $t_{GD} = 1000$, and $\delta = 0.001$ in our experiments.

Algorithm 2 Optimization Kernel

1: $m_0 \leftarrow 0$
2: $v_0 \leftarrow 0$
3: $t \leftarrow 0$
4: **while** $(\boldsymbol{x}, \boldsymbol{y})$ not converged **do**
5: $\quad t \leftarrow t + 1$
6: $\quad$ **if** $t \le t_{GD}$ **then**
7: $\quad\quad g_t \leftarrow \nabla f(\boldsymbol{x}, \boldsymbol{y})$
8: $\quad\quad m_t \leftarrow \beta_1 \cdot m_{t-1} + (1 - \beta_1) \cdot g_t$
9: $\quad\quad v_t \leftarrow \beta_2 \cdot v_{t-1} + (1 - \beta_2) \cdot g_t^2$
10: $\quad\quad \widehat{m}_t \leftarrow m_t / (1 - \beta_1^t)$
11: $\quad\quad \widehat{v}_t \leftarrow v_t / (1 - \beta_2^t)$
12: $\quad\quad (\boldsymbol{x}, \boldsymbol{y}) \leftarrow (\boldsymbol{x}, \boldsymbol{y}) - \alpha \cdot \widehat{m}_t / (\sqrt{\widehat{v}_t} + \epsilon)$
13: $\quad$ **else**
14: $\quad\quad (\boldsymbol{x}, \boldsymbol{y}) \leftarrow (\boldsymbol{x}, \boldsymbol{y}) - \delta \cdot \nabla f(\boldsymbol{x}, \boldsymbol{y})$

4.1.3 $\boldsymbol{\lambda}$ settings. The multipliers $\boldsymbol{\lambda}$ initialization and update schemes are important to the overall effectiveness of the global placement. Figure 5 illustrates the process of global placement for an operational amplifier. With guide from current flow and wirelength, the modules are efficiently spread out from the center (Fig. 5(b)). The overlapping and asymmetry penalty are emphasized in the later iterations to resolve the hard constraints (Fig. 5(b) and (c)). A significant challenge in global placement is that the problem scale and constraints vary in different circuits. The settings of multipliers $\boldsymbol{\lambda}$ essentially control and balance between different objectives and constraints. To smooth the constraint resolving and balance the objectives, we initialize and update $\boldsymbol{\lambda}$ as follows.

$\boldsymbol{\lambda}$ initialization: We initialize the $\boldsymbol{\lambda}$ by matching the L-2 norm of the gradients of each cost, as shown in Equation 14.

$$\lambda^{(0)} = \min\Big(\frac{\left\| \nabla_{\boldsymbol{x},\boldsymbol{y}} f^{SWL(0)} \right\|}{\left\| \nabla_{\boldsymbol{x},\boldsymbol{y}} f / \Phi^{(0)} \right\|}, \lambda_{MAX} \Big), \tag{14}$$

where $f^{SWF(0)}$ are initial SWF cost, $f/\Phi^{(0)}$ denotes initial values for other costs and λ_{MAX} is the maximum value allowed in initialization. We set $\lambda_{MAX} = 30$ in the experiments. Intuitively, matching the gradient norm motivates the optimization kernel to give similar efforts on each type of cost.

$\boldsymbol{\lambda}$ update: In the updating scheme, we intend to balance the optimization efforts to the objectives (SWL, PWL, SSF) and gradually emphasize the penalties (OVL, ASYM, CRF).

For the objectives (PWL/SSF), we match the cost gradient norm in early iterations and gradually converge the multipliers to constants, as shown in Equation 15.

$$\lambda^{(t)} = \zeta^t \cdot \frac{\left\| \nabla_{\boldsymbol{x},\boldsymbol{y}} f^{SWL(t)} \right\|}{\left\| \nabla_{\boldsymbol{x},\boldsymbol{y}} f^{(t)} \right\|} + \frac{w_*^{SWL}}{w_*}, \tag{15}$$

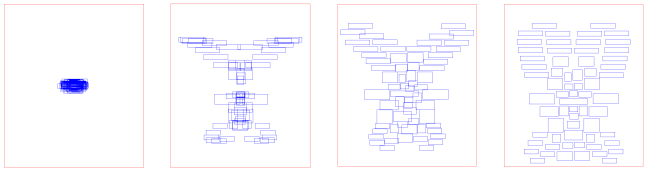
where $f^{(t)}$ is the current PWL/SSF cost, $f^{SWL(t)}$ is the current SWL cost, ζ is the decay rate, $f^{(t)}$ is the current PWL/ SSF cost, w_* is the total PWL/SSF weights and w_*^{SWL} is the total SWL weights. ζ is set to be 0.98 in the experiments.

For the penalties, we use subgradient method [13] to update the multipliers as shown in Equation 16.

$$\lambda^{(t)} = \lambda^{(t-1)} + \eta \cdot \Phi^{(t)}, \tag{16}$$

where $\Phi^{(t)}$ is the current OVL/ASYM/CRF cost and η is the step size. η is set to be 0.01 in the experiments.

Intuitively, we choose to balance the optimization efforts on each objective and let the penalties to be gradually increased over iterations.



(a) (b) (c) (d)

Figure 5: The intermediate results in global placement. (a) After initializing random placement. (b) After iteration 1. (c) After iteration 2. (c) After global placement terminates.

4.1.4 γ *settings.* The control parameters γ are used to control the trade-off between smoothness and accuracy in LSE function. The LSE approximation of the max min function is smoother with larger γ and more accurate for smaller γ [27]. Figure 6 shows an example of LSE approximation of $\max(x, 0)$ with different values of γ.

In early iterations, we use larger γ in OVL and CRF costs for providing a smoother function for the optimization. After the modules being spread out, we use smaller γ to obtain a more accurate $O^{OVL/CRF}$ overflow approximation to resolve the local violations. We update the γ_{OVL} and γ_{CRF} with a reciprocal function with respect to the penalty Φ^{OVL} and Φ^{CRF} respectively as shown in Equation 17.

$$\begin{aligned} \gamma^{(t)} &= -\frac{a}{\Phi^{(t)} - \kappa \cdot \Phi_*} + b, \\ a &= (\kappa^2 - \kappa) \cdot \Phi_* \cdot (\Gamma_H - \Gamma_L), \\ b &= (1 - \kappa) \cdot \Gamma_H + \kappa \cdot \Gamma_L, \end{aligned} \tag{17}$$

where $\Phi^{(t)}$ is the current penalty cost for OVL or CRF, Φ_* is the maximum OVL/CRF penalty cost, Γ_H/Γ_L are the maximum/minimum allowed values for γ and κ is a parameter to control the decay rate. Φ_* is estimated by setting it to the largest Φ^{OVL}/Φ^{CRF} observed so far in the iterations. κ is set to 100, Γ_H is set to 2, and Γ_L is set to 0.4 in the experiments. Equation 17 is essentially a reciprocal function mapping $[0, \Phi_*] \rightarrow [\Gamma_L, \Gamma_H]$. Empirically γ decays very fast as the overlapping and current flow penalties are handled efficiently after a few iterations.

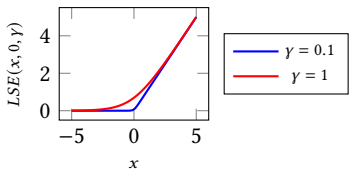


Figure 6: LSE approximation of $\max(x, 0)$ **with different** γ

4.2 Legalization

After the global placement stage, the modules have been placed considering wirelength and signal flow, with small or no violation of overlapping and asymmetry. We further compact the area of the layout and optimize for wirelength based on the method similar to [40].

Algorithm 3 Legalization

1: Construct the horizontal constraint graph $G_h := (\mathcal{M}, E_h)$
2: Area-driven symmetry-aware LP compaction on horizontal direction
3: Construct the vertical constraint graph $G_v := (\mathcal{M}, E_v)$
4: Area-driven symmetry-aware LP compaction on vertical direction
5: Wirelength-driven symmetry-aware LP detailed placement

Different from the approach with *missing positional relationships detection* techniques in [40], we separate the layout compaction on horizontal and vertical directions. As shown in Algorithm 3, we obtain the necessary positional relationships between modules based on the plane sweep line algorithm from [9] and represent them as edges in constraint graphs. Then we compact the layout with each edge being a linear constraint in LP problem to enforce non-overlapping between modules. Figure 7 shows an example of the constraint generation and area-driven compaction. As shown in Figure 7(b), we sweep the layout in horizontal, add a constraint edge between modules overlapping in y-coordinates (line 1 in Algorithm 3) and enforce the constructed constraint edges in the layout (line 2 in Algorithm 3). In constructing the horizontal constraint graph, we waive the edge between B and D because resolving the overlapping between them by moving D upwards causes less displacement compared to move B left or right. The positional relationship between B and D will be automatically handled by the following vertical direction compaction, as shown in Figure 7(c). The method above can preserve the optimality claimed in [40], while not need the missing positional detection techniques in [40] nor any additional overhead. With the construction of constraint graphs, the area-driven compaction and wirelength-driven detailed placement are preceded using the linear-programming (LP) formulations from [40]. This LP approach also honors symmetric constraints by imposing symmetry through the LP problem constraints. Note that the order to compact in horizontal or vertical direction is exchangeable. Due to the page limit, we omit the details.

5 EXPERIMENTAL RESULTS

The proposed AMS placement framework is implemented in C++, and the linear programming problems are solved with Gurobi [10]. All experiments are conducted on a Linux workstation with an 8-cores Intel 3.0 GHz CPU with 64 GB memory.

In the experiments, we conduct experiments with two complete mixed-signal systems, continuous-time ΔΣ modulators (CTDSM) denoted as ADC1 and ADC2 and three analog block-level circuits, one comparator and two operational amplifiers (OPs), denoted as COMP, OP1 and OP2. The five benchmark circuits vary in scale and functions and are designed by experienced circuit designers under TSMC 40nm process. Table 3 shows the benchmarks statistics.

For the two ADCs with hierarchical structures, we follow the hierarchy from the spice netlist, place each block separately and integrate the top-level circuits together with the blocks generated. This approach is similar to the manual design methodology of divide-and-conquer.

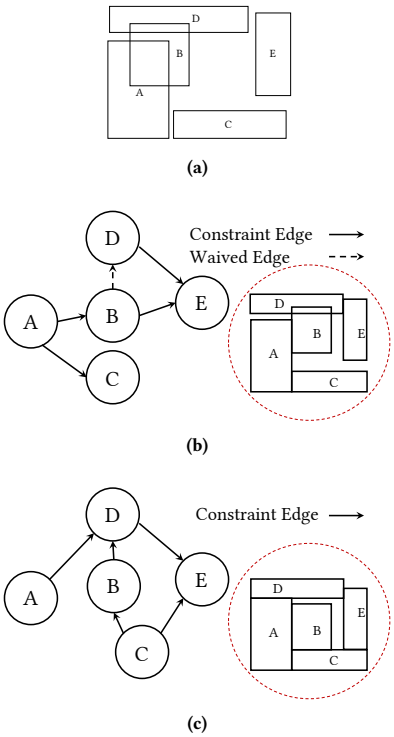


Figure 7: An example of the constraint graph construction and area-driven layout compaction. (a) A global placement result. (b) Horizontal constraint graph and the resulting layout after compaction. (c) Vertical constraint graph and the resulting layout after compaction.

Table 3: Benchmark circuits information of number of PMOS, number of NMOS, number of capacitors, number of resistors, number of standard cells, number of total modules, and number of symmetry constraints.

Benchmark	#PMOS	#NMOS	#Cap	#Res	#Stdcells	Total	#Sym
ADC1	29	32	16	24	11	112	57
ADC2	20	21	9	17	9	76	71
COMP	8	8	0	0	0	16	9
OP1	10	16	6	32	0	64	30
OP1	14	9	2	0	0	25	14

To evaluate the effectiveness of our proposed system signal flow-aware AMS placement framework, we compare to the state-of-the-art AMS placer [40]. We obtain the source code from the authors of [42] and modify the software as follows. Based on the guidance from the original designers of the benchmark circuits, we forbid the capacitors to be overlapped with transistors, because the benchmark circuits in the experiments are sensitive to the coupling.

To comprehensively illustrate the impact on routing, we use a detailed router aware of symmetry constraints to route every placement in the experiments. The used detailed router [5] will ensure the exact symmetry on matched nets specified by the circuit designers. The power and ground nets are routed with the approach similar to Figure 4 to ensure IR-drop does not impact the performance. The detailed router will strictly check the design rules. However, for the cases presenting exceeding routing congestion, it is possible that no feasible routing can be found with strict design rule checking and symmetry constraint handling. In such cases, to provide a meaningful comparison, we relax the design rule checking in the detailed routing and mark them in the tables. Within the experiments of this paper, all relaxed-design-rule routing results in design rule violations (DRV).

The routing wire width and the choice of VIAs are following the guidelines from the experienced designer in a net-by-net manner. We verify the routing quality with the designer that the overall routing is reasonable and shall not largely affect the fairness of comparisons. We verify the resulting layout with Calibre nmLVS and check the design rule with Calibre nmDRC.

Figure 1 shows the routed layout for ADC2 with our placement framework, where (b) is with system signal flow, and (c) is without system signal flow.

5.1 Experimental results on placement metrics

We evaluate and compare the placement results on area, HPWL, routed wirelength, number of vias used in routing and runtime. The average of multiple runs collect all the runtime.

Table 4 shows the comparisons on the results of three analog block-level circuits. We achieve 34%, 23%, and 10% reductions in area, routed wirelength and number of VIAs over [40] with comparable runtime. Note that these results are obtained with OP2 not routable with strict design rule.

On the other hand, Table 5 shows the comparisons on two ADCs. As shown in Figure 1, honoring the system signal flow will likely result in a larger area and longer wirelength, however, the proposed placement framework still outperform [40] in routed wirelength and number of VIAs by 20% and 23% respectively. The proposed framework without system signal flow can further enlarge the gap in routed wirelength to 36% with a similar area. Note that both of the two ADCs are failed in routing with strict design rules for [40].

Our placement framework achieve 4.2%, 35.8% and 16.4% reduction in area, routed wirelength and number of VIAs respectively without system signal flow. With system signal flow, our placement increase area by 7.3% while reduce routed wirelength and number of VIAs by 22.8% and 19.5%, combining the results from five benchmark circuits.

We can notice that the lower HPWL in OP2 with [40] does not results in lower routed wirelength. It is because the wirelength for P/G nets are significantly longer than HPWL estimation.

5.2 Experimental results on performance

To verify the results on circuit performance, we conduct post-layout simulations. Calibre PEX is used to extract the parasitic resistance, parasitic capacitor, and coupling capacitance (R+C+CC). Then the performance is evaluated with Cadence Spectre.

Table 6 illustrates the effectiveness of system signal flow, where SNDR, SFDR, THD, ENOB denote for signal-to-noise-and-distortion ratio, spurious-free dynamic range, total harmonic distortion and effective number of bits, respectively. Since the comparisons differ only in whether consider system signal flow in top-level of integrating the system, the block-level circuits in the two ADCs are exactly the same. Hence the difference in performance comes purely on the floorplan in the top-level integration. With system signal flow, the post-layout SNDR is improved by 2.2 dB and 6.7 dB, respectively. Figure 8 shows the simulation results for ADC2. We can observe that the layout with optimized signal flow has lower harmonic distortion. The improvements in post-layout performance for two ADCs demonstrates the importance of the parasitic RC along the critical signal path and the effectiveness of the "place-like-schematic" approach in planning the signal flow in placing mixed-signal systems.

Table 4: Comparison of area(μm^2), half-perimeter wirelength (HPWL(μm)), routed wirelength (RWL(μm)), number of VIAs (VIA), number of design rule violations (DRV), 1-thread runtime (1-T RT(s)) and 8-thread runtime(8-T RT(s)) for block-level analog circuits.

CKTS	[40]						This Work						
	Area	HPWL	RWL	VIA	DRV	1-T RT	Area	HPWL	RWL	#VIA	DRV	1-T RT	8-T RT
COMP	223	104	267	21	**0**	0.16	**187**	**101**	**196**	**13**	**0**	0.18	**0.08**
OP1	2366	767	1234	97	**0**	3.3	**1584**	**691**	**905**	**84**	**0**	14.59	**3.09**
OP2	2529	**416**	914	**44**	14†	**0.14**	**2047**	466	**732**	50	**0**	9.63	2.73
Ratio	1.34	1.02	1.23	1.10	-	**0.61**	**1.00**	**1.00**	**1.00**	**1.00**	-	4.79	1.00

† Routing fails with strict design rules

Table 5: Comparison of area(μm^2), half-perimeter wirelength (HPWL(μm)), routed wirelength (RWL(μm)), number of VIAs (VIA), number of design rule violations (DRV), 1-thread runtime (1-T RT(s)) and 8-thread runtime(8-T RT(s)) for two mixed signal system circuits.

CKTS	[40]						Without SSF							With SSF						
	Area	HPWL	RWL	VIA	DRV	1-T RT	Area	HPWL	RWL	VIA	DRV	1-T RT	8-T RT	Area	HPWL	RWL	VIA	DRV	1-T RT	8-T RT
ADC1	11840	2402	3817	297	45†	**1.64**	**10720**	**2401**	**2909**	**247**	**0**	10.65	2.74	11170	2691	3154	255	**0**	10.51	2.70
ADC2	**22800**	4103	4290	252	157†	1.23	23620	**3032**	**3004**	217	**0**	0.85	**0.64**	27670	3415	3580	**193**	**0**	1.05	0.68
Ratio	0.89	1.07	1.20	1.23	-	**0.85**	**0.88**	**0.89**	**0.88**	1.04	-	3.40	1.00	1.00	1.00	1.00	**1.00**	-	3.42	1.00

† Routing fails with strict design rules

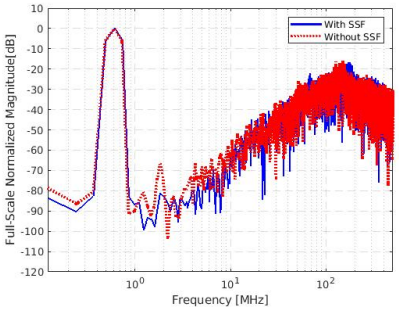


Figure 8: Simulation results on ADC2 with and without system signal flow.

Table 6: Comparisons of post-layout simulations results with and without the system signal flow in mixed-signal system circuits. ADC1/ADC2 has sampling frequency of 320/1000 MHz and bandwidth of 2.5/6.25 MHz.

Circuits		Schematic	Without SSF	With SSF
ADC1	SNDR (dB)	66.2	61.4	63.6
	SFDR (dB)	78.9	75.0	77.1
	THD (dB)	75.0	70.6	73.8
	ENOB (bits)	10.70	9.90	10.27
	Power (mW)	0.837	0.864	0.870
ADC2	SNDR (dB)	67.1	59.6	66.3
	SFDR (dB)	82.0	67.0	80.2
	THD (dB)	77.6	66.5	76.4
	ENOB (bits)	10.85	9.61	10.71
	Power (mW)	0.677	0.740	0.757

Table 7: Post-layout simulations results of our AMS placement framework. ADC1/ADC2 has sampling frequency of 320/1000 MHz and bandwidth of 2.5/6.25 MHz.

Circuits		Schematic	[40]	This work
ADC1	SNDR (dB)	66.2	60.2	63.6
	SFDR (dB)	78.9	72.0	77.1
	THD (dB)	75.0	68.8	73.8
	ENOB (bits)	10.70	9.70	10.27
	Power (mW)	0.837	0.877	0.870
ADC2	SNDR (dB)	67.1	56.3	66.3
	SFDR (dB)	82.0	66.7	80.2
	THD (dB)	77.6	66.2	76.4
	ENOB (bits)	10.85	9.06	10.71
	Power (mW)	0.677	0.790	0.757
COMP	Delay (ps)	103	187	157
	Offset (μV)	-	90	380
	Noise (μV_{rms})	439.8	360.1	368.8
	Power (μW)	13.45	21.82	21.51
OP1	DC Gain (dB)	53.95	45.53	54.13
	Bandwidth (MHz)	612.6	396.0	389.7
	Phase Margin (°)	50.65	63.05	65.83
	Offset (μV)	-	1553	448
	CMRR (dB)	-	83.32	118.7
	Power (μW)	374.3	377.3	377.9
OP2	DC Gain (dB)	38.20	37.65	37.73
	Bandwidth (MHz)	110.5	97.19	94.48
	Phase Margin (°)	64.66	70.67	67.76
	Offset (μV)	-	3845	151
	CMRR (dB)	-	71.13	219.9
	Power (μW)	776.6	778.2	757.6

Table 7 shows the complete post-layout simulation results compared to [40]. In addition to the 10 dB SNDR advantage in ADC2 over the baseline, our placement framework consistently achieves satisfying performance in all the five benchmark circuits.

In fact, the ADC2 chip implemented with the proposed framework using TSMC 40nm technology has been sent to the foundry for tape-out.

6 CONCLUSION

This work presents a new performance-driven placement framework for AMS circuits. The proposed framework considers the system signal flow in mixed-signal systems and planning the signal path in a "place-like-schematic" approach. The proposed self-adaptive global placement engine balance the different objectives and constraints in AMS placement problem. Experimental results have demonstrated the effectiveness of system signal flow in mixed-signal system performance and the sign-off quality of placement results from the proposed framework.

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